PATENT ABSTRACTS OF JAPAN

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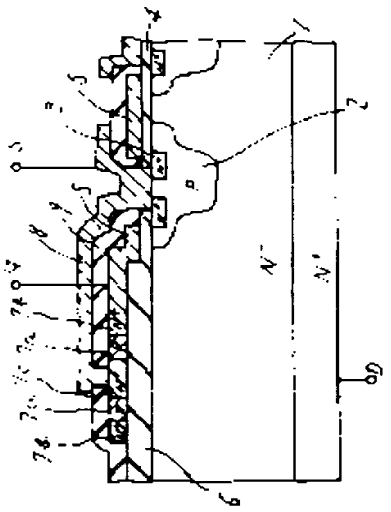
(54) INSULATING GATE TYPE SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To obtain a vertical MOSFET advantageous for preventing electrostatic breakdown by electrically connecting an internal impurity introducing layer to a source and integrally connecting an external impurity introducing layer to a semiconductor gate.
CONSTITUTION: Since structure in which an internal N+ diffusion region 7c surrounded by a looped PN junction is connected to a source electrode and an external N+ diffusion region 7b is connected to a gate electrode is formed in a back-to-back protective diode using a polycrystal Si layer, the protective diode can be formed at the arbitrary position of the substrate of the MOSFET, size and shape can freely be selected as compared to the case when a slender NPN junction is shaped along the periphery of the substrate as seen in the conventional devices, and a layout is also extremely easy. Electrostatic breakdown can effectively be prevented by forming such a protective diode in parallel between the gate and the source.



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